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Modular symmetric and asymmetric reduced count switch multilevel current source inverter

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Abstract: Current source inverters (CSIs) have prominent features compared to voltage source inverters. The CSIs are less affected by grid voltage fluctuations, their control is simple and they have inherent short-circuit protection. This study proposes a novel multilevel CSI based on modular cells. The proposed topology is performed based on the parallel connection of two-switch modules. According to the value of current sources in each module, the proposed configuration can be operated in two modes of operation: symmetric and asymmetric. A comparison study is carried out between the proposed topology, the cascaded H-bridge and a recently developed topology in terms of the number of switches, the number of sources, total switch device power, and power losses. The comparison study shows a great improvement in performance of the proposed symmetric and asymmetric topologies compared to conventional structures. In addition, the proposed circuit shows an interesting feature which is the common emitter connection of the main switches. This arrangement leads to simple gate drive circuits. Finally, seven-level symmetric topology and fifteen-level asymmetric topology are simulated and the laboratory prototypes of them are implemented. The presented simulation and experimental results validate the feasibility of proposed topologies.

1 Introduction

Nowadays evolution of high-performance semiconductor power electronic devices, such as metal-oxide semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT), integrated gate-commutated thyristor (IGCT), dual gate commutated thyristor (dual GCT), and emitter turn-off thyristors (ETOs) have caused various research trends in high-power converters, such as multilevel inverters [1, 2]. Lower total harmonic distortion (THD) and stress on inductors and switches, reduced dv/dt or lower di/dt in high-power applications and reduced electromagnetic interference (EMI) noise are the substantial advantages of multilevel inverters [3, 4].

Multilevel converters are classified into two groups: multilevel voltage source inverters (MVSIs) and multilevel current source inverters (MCSIs). Several papers published to improve MVSIs in the number of devices, the number of voltage levels, power rating and so on [5, 6]. However, a little attention has been devoted to MCSIs while they have more advantages in comparison with MVSIs [7, 8]. In addition, they are one of the best solutions to tackle inverter output current harmonic and THD of inverter, imposed by various international standards, like IEEE-1547, IEEE-929. In high power industrial applications, in which low voltage and high current are required, such as induction motor drives [4], static reactive power compensation [9], power systems [10], and grid integration of renewable sources [11], MCSIs show reliable operation. Moreover, there are no requirement to overcurrent and the short-circuit protection in MCSIs [7].

Several MCSI topologies have been developed in the literature [8, 12–18]. Paralleling three-level H-bridge current source inverter (CSI) cells, which is called CHB (cascaded H-bridge) in this paper, is the simplest method to generate the multilevel current waveform [8]. Requirement of bulky and costly transformers in order to generate isolated DC current sources are the main drawbacks of this topology. Single-rating inductor and multi-rating inductor MCSI are introduced in [12]. Cumbersome inductor and complexity of control system to the balance inductor's current are the main problems associated with these configurations. Although, several authors tried to balance the inductor current, reported in [13], but the requirement to bulky inductor has remained. In [14], three-level MCSI parallel with two-level CSI was presented. The requirement to multiple isolated DC current sources and complex control algorithm were the disadvantages of this topology. These authors proposed another variant MCSI using inductor cell connected to H-bridge. Unlike parallel MCSI, this topology does not require multiple isolated DC current sources and complexity of control method is moderated. However, costly, high volume, and multi rating inductor still exist [15]. A new circuit configuration of single-phase MCSI was proposed in [16]. In this structure, a basic H-bridge CSI working as the main inverter generates a multilevel current waveform in cooperation with inductor cells connected in parallel. Each inductor cell is composed of four unidirectional power switches across with an inductor across the cell circuit. The aim of inductor cells is to generate the intermediate levels of output waveform with no additional external DC-power sources. However, regulating the magnitude of inductor currents is the main disadvantage of this circuit, especially when the number of inductor cells is increased. Similarly, using inductor cells paralleled with H-bridge converter was presented in [17]. Each inductor cell is composed of four switches and two inductors. Bulky inductors are used to obtain smooth DC currents. Regulating the inductor currents and the existence of discrete diodes connected in series with the power switches are some drawbacks associated with the CSI topology, which often degrade its efficiency [13]. In [18], a novel grid-connected multilevel CSI was proposed. This circuit not only operates under low photovoltaic panel voltage, due to the boosting capability of the employed CSI topology, but also a low THD at low switching frequency is obtained due to the multilevel operation. In CSIs, disconnection may destroy the whole system; therefore, it is important to take a strategy to prevent from this issue.

This paper proposes a new configuration based on two-switch modules and H-bridge converter. Regards to the value of the current sources in the modules, symmetric and asymmetric structures are achieved. Proper connection of basic modules generates the positive current levels and an H-bridge converter is

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used to provide negative levels. One of the interesting features of the presented topology is the common emitter connection of main switches which lead to simple gate drive circuit. Moreover, the number of switches, the number of current sources, and power losses are examined and comparison study shows that the proposed topologies have better performance in terms of the number of current sources, power losses, and the number of IGBTs.

This paper is organised as follows: in Section 2, the structure of the proposed multilevel converter based on module cells is introduced and simulation results of symmetric and asymmetric topologies are carried out. Comparison study is performed in Section 3. Experimental results are given in Section 4, and finally some conclusions are drawn in Section 5.

2 Proposed current source multilevel inverter

In this section, a novel MCSI topology is proposed. The main feature of MCSIs is the requirement of unidirectional current switches which can be implemented by single diode-less IGBT or IGBT/diode (or MOSFET) with a series connected diode. Also, an AC capacitor must be connected in parallel with load in MCSIs. This capacitor not only plays filter role in MCSIs but also protect the converters against current step changes of current due to the existence of inductive component in output current.

The proposed topology has all of general features of conventional MCSIs. In addition, the proposed topology has a factor of merits, such as reduced the number of components, lower number of DC current sources, and lower implementation cost due to common-emitter connection of IGBTs, compared to conventional structures.

Considering the value of current sources, the proposed topology can be operated in symmetrical and asymmetrical structures. In symmetrical type, values of DC current sources are equal; in addition, in asymmetrical one, their values should be different. These two cases are detailed as follows.

2.1 Operation principle of symmetrical mode

Fig. 1 shows the proposed symmetrical structure which all of current sources have the same values. As it can be seen from Fig. 1, the presented structure is formed by connection of basic 'current cells' and the H-bridge converter. Each current cell is composed of a DC current source and two power electronic switches (IGBTs) in which they turn on and off in a complimentary manner. One of the IGBTs is paralleled with DC current source. When this switch is turned on, the DC source is trapped in the circuit loop and this cell does not participate in the output levels. Otherwise, the current cell injects the DC source to the output.

Assuming that the maximum output current is I_{DC}, in order to generate symmetrical steps in output current, amplitude of current sources should be considered as follows

$$\begin{cases} I_{DC,1} = I_{DC,2} = \cdots = I_{DC,N_{Source}} \\ I_{DC,i} = \dfrac{I_{DC}}{N_{Source}} \quad i = 1, \ldots, N_{Source} \end{cases} \tag{1}$$

where N_{Source} is the number of DC current sources. Each current source can be realised by series connection of a DC voltage source and an inductor. The value of current source is controlled via controlling DC voltage source controlling. It should be noted that a freewheeling diode must be paralleled with series connection of DC voltage source and switch as shown in Fig. 1.

Fig. 1 illustrates that in the proposed topology, positive levels are generated by paralleling the basic cells, and the negative levels are produced by the H-bridge converter in which the switching frequency is low. The relation between the number of output current levels (N_{Level}) and the number of unidirectional semiconductor switches (N_{IGBT}) can be formulated as follows

$$N_{Level} = N_{IGBT} - 3 \tag{2}$$

In addition, in order to generate N_{Level} steps in the output current, the number of current sources is given as below

$$N_{Source} = \frac{N_{Level} - 1}{2} = \frac{N_{IGBT} - 4}{2} \tag{3}$$

If the zero level is generated using an H-bridge, then two unidirectional switches of the last module can be eliminated and the improved symmetric structure is achieved as shown in Fig. 2.

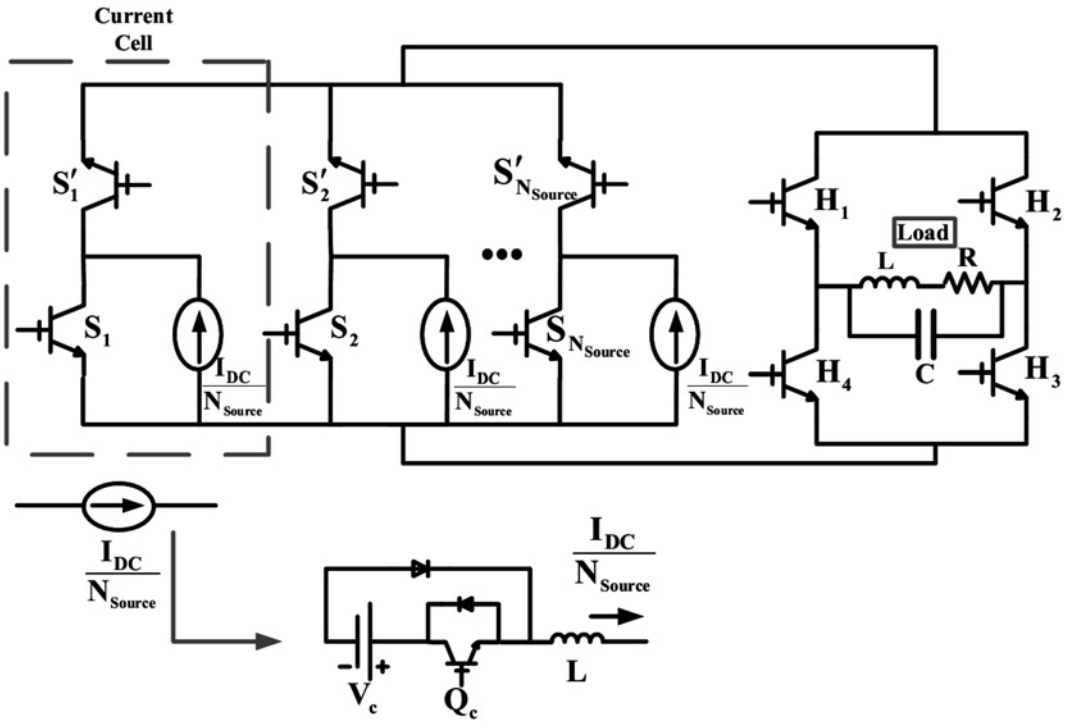

Fig. 1 *Proposed symmetrical structure*

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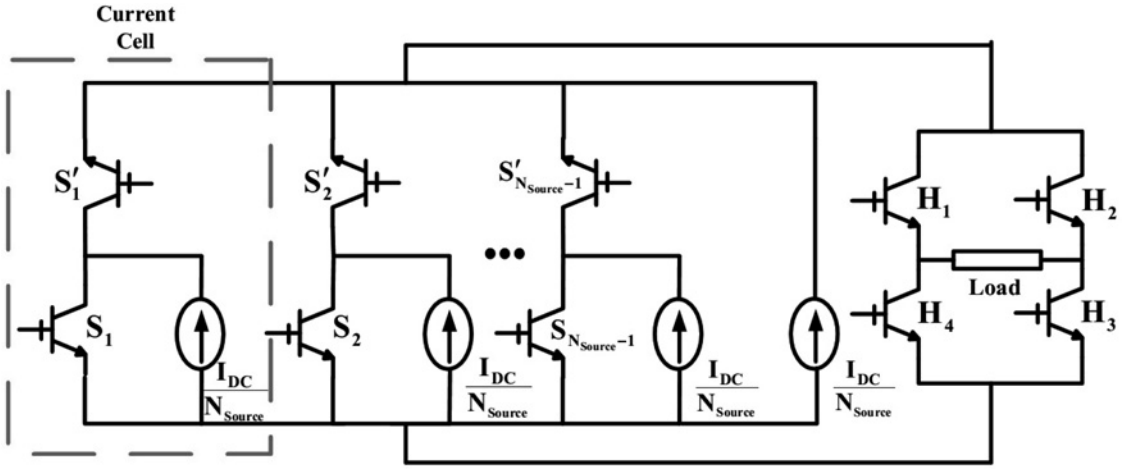

Fig. 2 *Modified proposed symmetrical structure*

Therefore, the following equations can be rewritten for the improved symmetric topology

$$N_{\text{Level}} = N_{\text{IGBT}} - 1 \tag{4}$$

$$N_{\text{Source}} = \frac{N_{\text{Level}} - 1}{2} = \frac{N_{\text{IGBT}} - 2}{2} \tag{5}$$

The switching states of improved proposed converter are listed in Table 1. By implementing the switching table and the level shifted pulse-width modulation (LS-PWM) technique, the proposed converter is controlled as shown in Fig. 3. With comparing a sinusoidal reference waveform and level shifted carrier signals the desired positive levels of desired output current levels are generated and negative levels are produced via an H-bridge converter.

Table 1 Switching states of proposed MCSI in symmetrical mode

Current level	Switching states										
	S_1	S_1'	S_2	S_2'	⋯	S_{N-1}	S_{N-1}'	H_1	H_2	H_3	H_4
$-I_{DC}$	0	1	0	1		0	1	0	1	0	1
$-((N_{Source}-1)I_{DC})/N_{Source}$	1	0	0	1		0	1	0	1	0	1
$-((N_{Source}-2)I_{DC})/N_{Source}$	1	0	1	0		0	1	0	1	0	1
⋮								0	1	0	1
$-(I_{DC}/N_{Source})$	1	0	1	0		1	0	0	1	0	1
0	1	0	1	0		0	1	1	1	1	1
I_{DC}/N_{Source}	1	0	1	0		1	0	1	0	1	0
⋮								1	0	1	0
$((N_{Source}-2)I_{DC})/N_{Source}$	1	0	1	0		0	1	1	0	1	0
$((N_{Source}-1)I_{DC})/N_{Source}$	1	0	0	1		0	1	1	0	1	0
I_{DC}	0	1	0	1		0	1	1	0	1	0

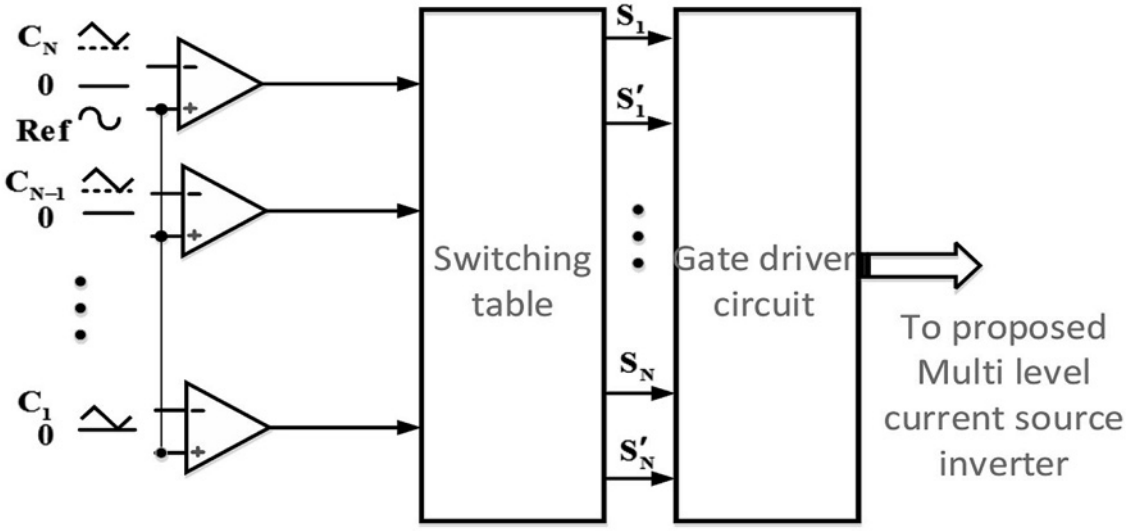

Fig. 3 *LS-PWM scheme for proposed converter*

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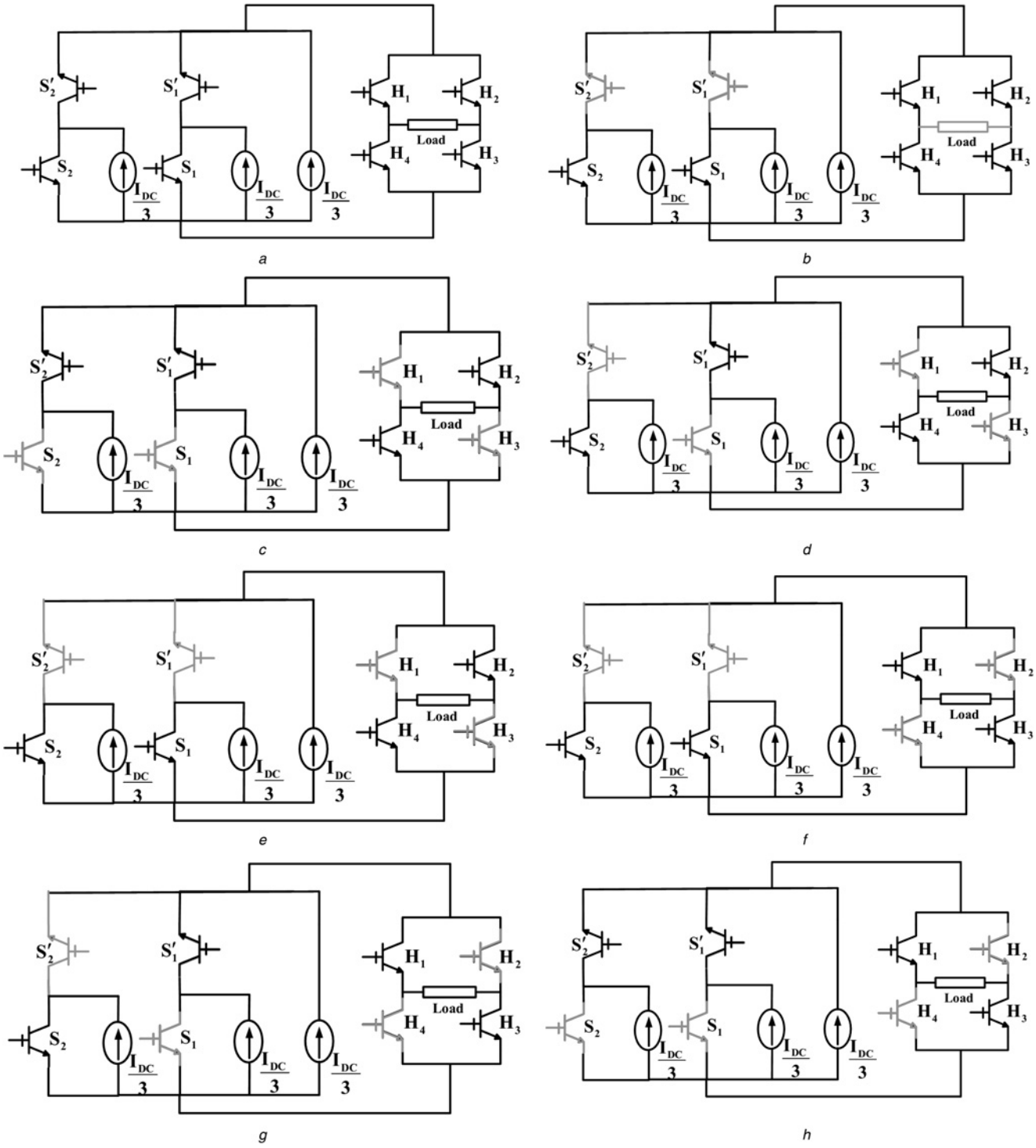

Fig. 4 *Modified proposed seven-level MCSI*

a Circuit diagram
b Zero-level equivalent circuit
c I_{DC}-level equivalent circuit
d $2I_{DC}/3$-level equivalent circuit
e $I_{DC}/3$-level equivalent circuit
f $-I_{DC}/3$-level equivalent circuit
g $-2I_{DC}/3$-level equivalent circuit
h $-I_{DC}$-level equivalent circuit

The $N_{Level} = 7$ is considered for a case study in order to obtain seven-level output currents: $-I_{DC}$, $-2(I_{DC}/3)$, $-(I_{DC}/3)$, 0, $I_{DC}/3$, $2(I_{DC}/3)$, and I_{DC}. According to (4) and (5), three DC current sources and eight IGBTs are employed. Four of switches are used to generate the three basic positive levels (I_{DC}, $2(I_{DC}/3)$, and $I_{DC}/3$) and other four switches belong to the H-bridge as shown in Fig. 4*a*. Figs. 4*b*–*h* illustrate equivalent circuits to generate the various current levels. Also switching states of proposed seven-level MCSI in symmetrical mode are extracted from Table 1, and listed in Table 2.

Simulation results of modified proposed seven-level symmetric CSI is depicted in Fig. 5. The value of each current source,

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Table 2 Switching states of improved proposed seven-level MCSI in symmetrical mode

Current level	Switching states							
	S_1	S'_1	S_2	S'_2	H_1	H_2	H_3	H_4
$-I_{DC}$	0	1	0	1	0	1	0	1
$-2(I_{DC}/3)$	0	1	1	0	0	1	0	1
$-I_{DC}/3$	1	0	1	0	0	1	0	1
0	1	0	1	0	1	1	1	1
$I_{DC}/3$	1	0	1	0	1	0	1	0
$2(I_{DC}/3)$	0	1	1	0	1	0	1	0
I_{DC}	0	1	0	1	1	0	1	0

modulation index, and the load are considered 0.35 A, 1, and 30 + j3.14 Ω, respectively.

2.2 Operation principle of asymmetrical mode

For the proposed asymmetrical MCSI, the values of DC current sources for each cell are different which are depicted in Fig. 6. To achieve the maximum levels in output current, the value of each current source should be chosen as follows

$$I_{DC,i} = \frac{2^{i-1}}{2^{N^*_{Source}} - 1} \tag{6}$$

where $I_{DC,i}$ is the value of the ith cell's DC current source and I_{DC} is the maximum output current. Therefore, the following equation exhibits the maximum value of the output current for the proposed asymmetric topology

$$I_{O,max} = \frac{I_{DC}}{2^{N^*_{Source}} - 1} \sum_{i=1}^{N^*_{Source}} 2^{i-1} = I_{DC} \tag{7}$$

Moreover, the relation between the number of output levels (N^*_{Level}) and the number of IGBTs (N^*_{IGBT}) is

$$N^*_{Level} = 2^{(N^*_{IGBT}-2)/2} - 1 \tag{8}$$

In other words, to generate N^*_{Level} steps, the N^*_{Source} and N^*_{IGBT} can be obtains as follows

$$N^*_{Source} = \log_2(N^*_{Level} + 1) - 1 \tag{9}$$

$$N_{IGBT} = 2[\log_2(N^*_{Level} + 1) + 1] \tag{10}$$

For example, if N_{Level} is selected 15, hence, according to (8)–(10), the number of DC current sources and IGBTs are calculated

$$N^*_{Source} = \log_2(15 + 1) - 1 = 3 \tag{11}$$

$$N^*_{IGBT} = 2[\log_2(15 + 1) + 1] = 10 \tag{12}$$

Fig. 7 shows the proposed fifteen-level asymmetric topology which switching states of this mode are listed at Table 3. Similar to symmetrical mode, LS-PWM scheme (Fig. 3) can be implemented by considering Table 3. Also, the simulation results for fifteen-level asymmetric topology are shown in Fig. 8. The values of current source cells are 0.35, 0.7, and 1.4 A, the modulation index and the load are 1 and 30 + j3.14 Ω, respectively.

2.3 Design of output filter capacitor

As mentioned the output filter capacitor, plays two key roles in CSIs:

(i) The harmonic components of the pulse-width modulation current will flow through the filter capacitor.

(ii) Due to existence of inductive load, the filter capacitor is required to avoid from the sudden current changes.

In addition, because the inverter behaves as a current source, so the total impedance connected to the output of CSI should be a capacitive. Regarding the equivalent circuit of output stage, which shown in Fig. 9, the size of capacitor is calculated as follows

$$(R + R_C)\left(R_C\omega L - \frac{R}{\omega C}\right) \le \left(\omega L - \frac{1}{\omega C}\right)\left(RR_C + \frac{L}{C}\right) \tag{13}$$

Equation (14) defines the resonance frequency of the output stage. The filter capacitor must be chosen in such a way that (14) is not satisfied

$$f_o = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{R^2C - L}{R_C^2C - L}} \tag{14}$$

3 Comparison study

In this section, the proposed topology in symmetrical and asymmetrical modes is compared with conventional structures. The symmetrical topology is compared to symmetric CHB converter and the topology that presented in [15]. Also, asymmetrical topology is compared to asymmetric CHB and the presented topology in [16]. Comparison indices are the number of semiconductor devices, the number of DC current sources, semiconductor device power (SDP), and total losses.

3.1 Symmetrical topologies

A desired multilevel inverter should be had fewer number of semiconductor devices, lower SDP, fewer number of DC sources, and lower losses in compared with other structures at same output levels. The detailed comparison study is depicted in Fig. 10. It is clear that the proposed structure has lower number of IGBTs rather than CHB and equal to [15] (see Fig. 10*a*). It should be noted that the presented topology in [15] has the same number of IGBTs but it needs two diodes in each cell. Another comparison index is the number of DC current sources which is the same number for the proposed topology and CHB, but [15] needs more.

To determine the losses a brief review of loss calculations are required. Commonly, the power loss of power electronic converters is mainly emanated from two factors:

(i) Conduction losses: This is produced due to the presence of equivalent resistance and the on-state voltage drop of the semiconductor power devices.
(ii) Switching losses: non-ideal characteristic of power switches is the origin of these losses.

Loss calculation of the suggested multilevel converter is illustrated in the following.

3.1.1. Conduction losses: In order to calculate the conduction losses, it is essential to evaluate the losses of one typical power switch and a diode then the approach should be generalised to overall system. The following relations are used to evaluate the conduction losses of switches and diodes, respectively [5]

$$P_{C,T}(t) = [V_T + R_T i^{\beta}(t)]i(t) \tag{15}$$

$$P_{C,D}(t) = [V_D + R_D\, i(t)]i(t) \tag{16}$$

where V_T and V_D are the on-state voltages of the transistor and the diode, R_T and R_D are the equivalent resistances of the transistor and the diode, and β is a constant related to the characteristic of the transistor.

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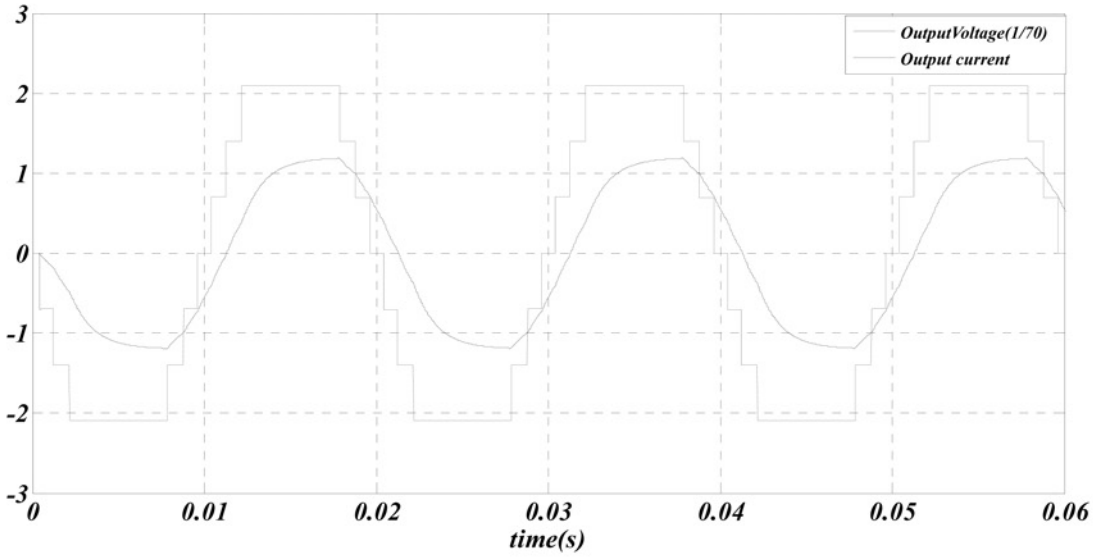

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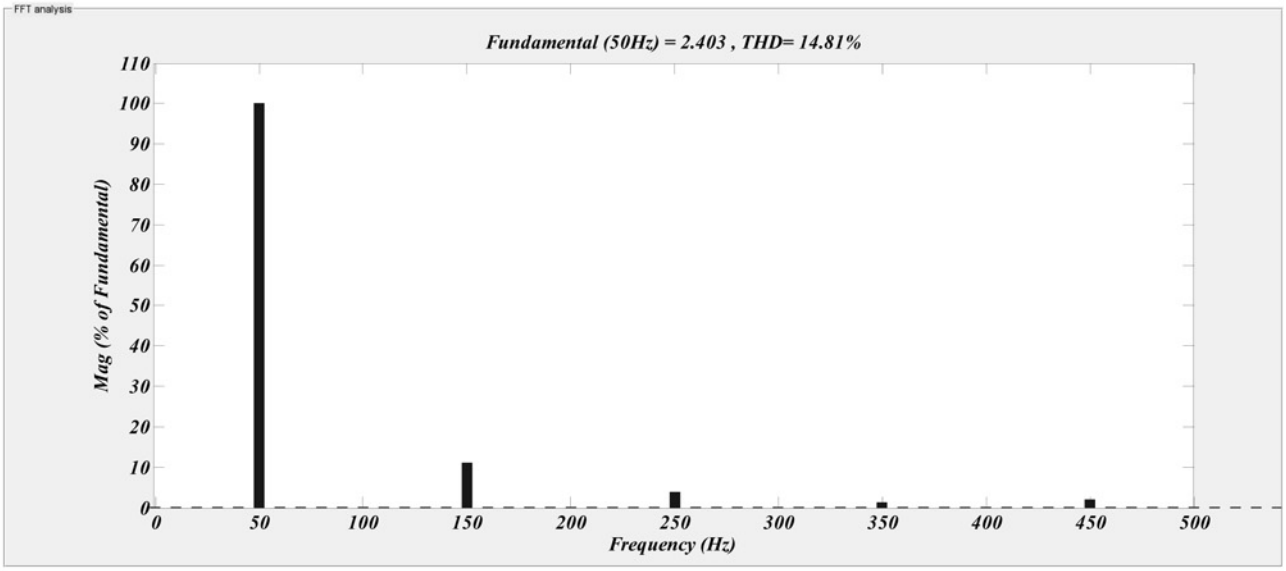

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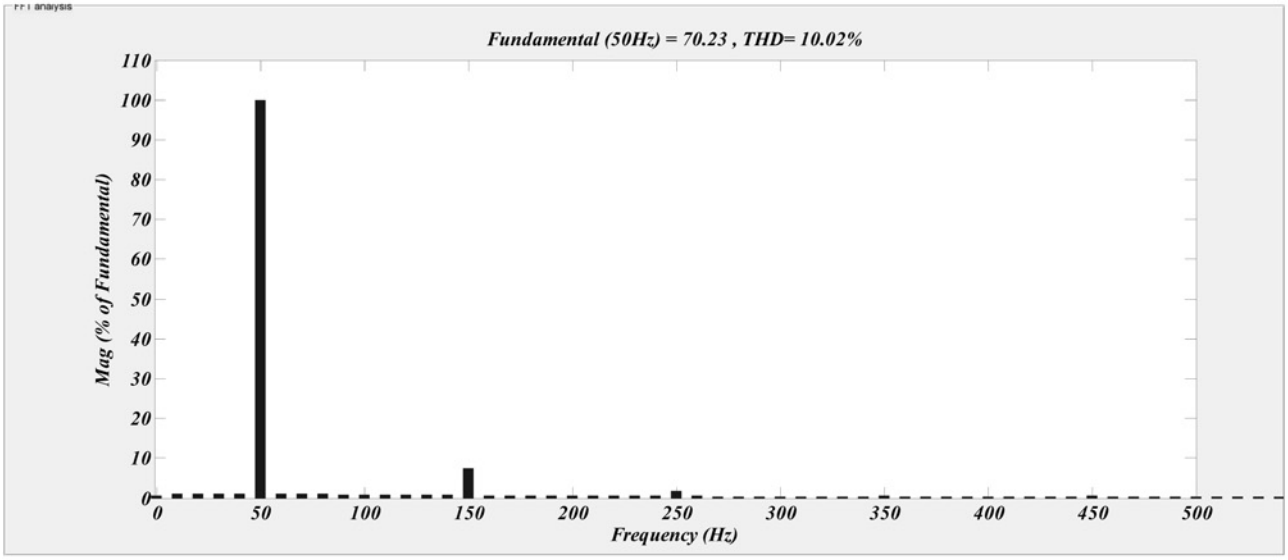

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Fig. 5 *Simulation results of the modified proposed seven-level symmetric topology*

a Load voltage and output current
b Harmonic spectrum of output current
c Harmonic spectrum of load voltage

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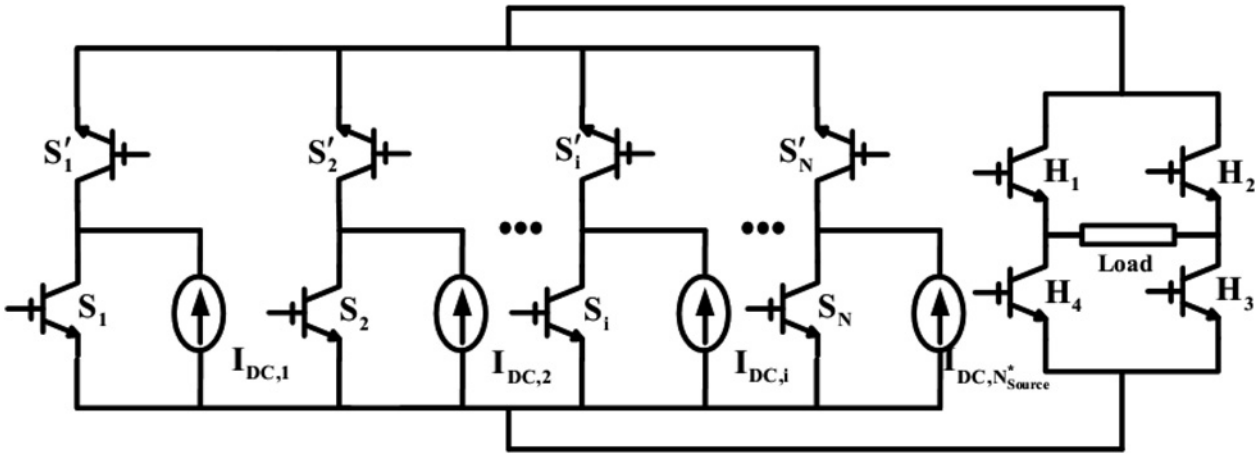

Fig. 6 *Proposed asymmetrical structure*

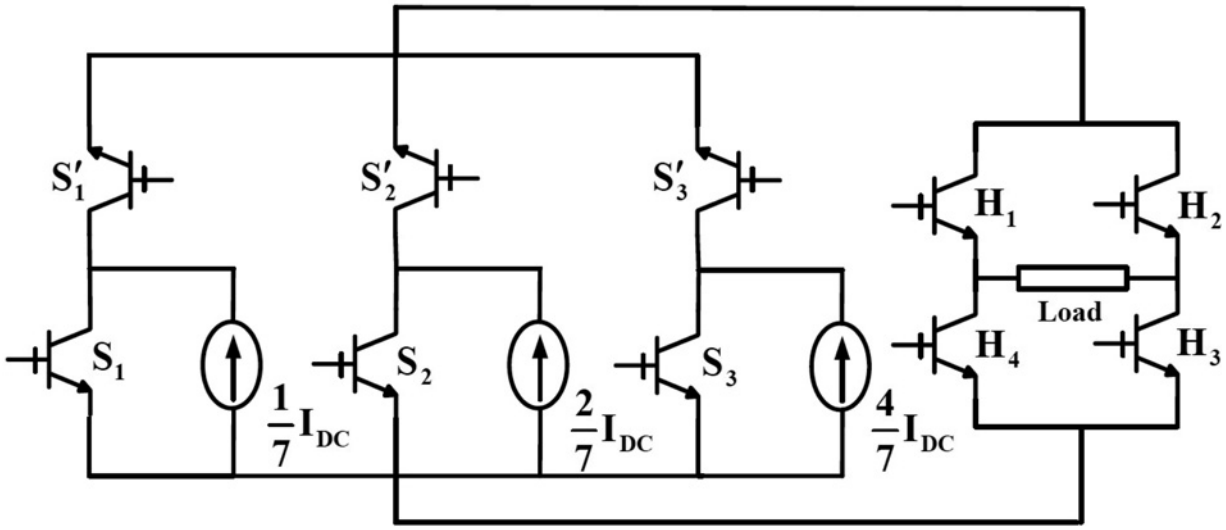

Fig. 7 *Proposed asymmetrical fifteen-level structure*

If we define that $x(t)$ and $y(t)$ are the number of transistors and diodes in the current path in any instant of time, respectively, using (15) and (16), the average conduction power loss of the proposed multilevel inverter can be obtained from the following expression [5]

$$P_{\mathrm{C}}(t) = \frac{1}{\pi}\int_0^{\pi} [(x(t)V_{\mathrm{T}} + y(t)V_{\mathrm{D}} + x(t)R_{\mathrm{T}}i^{\beta}(t) + y(t)R_{\mathrm{D}}i(t))i(t)]\,\mathrm{d}\omega t \tag{17}$$

Table 3 Switching states of proposed fifteen-level MCSI in asymmetrical mode

Current level	Switching states									
	S_1	S'_1	S_2	S'_2	S_3	S'_3	H_1	H_2	H_3	H_4
$-I_{\mathrm{DC}}$	0	1	0	1	0	1	0	1	0	1
$-(6I_{\mathrm{DC}}/7)$	1	0	0	1	0	1	0	1	0	1
$-(5I_{\mathrm{DC}}/7)$	0	1	1	0	0	1	0	1	0	1
$-(4I_{\mathrm{DC}}/7)$	1	0	1	0	0	1	0	1	0	1
$-(3I_{\mathrm{DC}}/7)$	0	1	0	1	1	0	0	1	0	1
$-(2I_{\mathrm{DC}}/7)$	1	0	0	1	1	0	0	1	0	1
$-I_{\mathrm{DC}}/7$	0	1	1	0	1	0	0	1	0	1
0	1	0	1	0	1	0	0	1	0	1
$I_{\mathrm{DC}}/7$	0	1	1	0	1	0	1	0	1	0
$2I_{\mathrm{DC}}/7$	1	0	0	1	1	0	1	0	1	0
$3I_{\mathrm{DC}}/7$	0	1	0	1	1	0	1	0	1	0
$4I_{\mathrm{DC}}/7$	1	0	1	0	0	1	1	0	1	0
$5I_{\mathrm{DC}}/7$	0	1	1	0	0	1	1	0	1	0
$6I_{\mathrm{DC}}/7$	1	0	0	1	0	1	1	0	1	0
I_{DC}	0	1	0	1	0	1	1	0	1	0

3.1.2 Switching losses: The switching losses are computed for an identical power switch and then the results are generalised for the suggested CSI. The total switching power losses is composed by two elements:

(i) IGBT switching power loss.
(ii) Anti-parallel diode power losses.

The following expressions can be given

$$P_{\mathrm{sw,T}} = (E_{\mathrm{on,T}} + E_{\mathrm{off,T}})f_{\mathrm{sw}} \tag{18}$$

$$\begin{aligned} P_{\mathrm{sw,Anti-D}} &= (E_{\mathrm{on,Anti-D}} + E_{\mathrm{off,Anti-D}})f_{\mathrm{sw}} \\ P_{\mathrm{sw,Anti-D}} &\simeq E_{\mathrm{on,Anti-D}}f_{\mathrm{sw}} \end{aligned} \tag{19}$$

where switching power losses of an IGBT are indicated as $P_{\mathrm{sw,T}}$, $E_{\mathrm{on,T}}$ and $E_{\mathrm{off,T}}$ are turn on energy and turn off energy losses in IGBT, respectively, and f_{sw} is the switching frequency.

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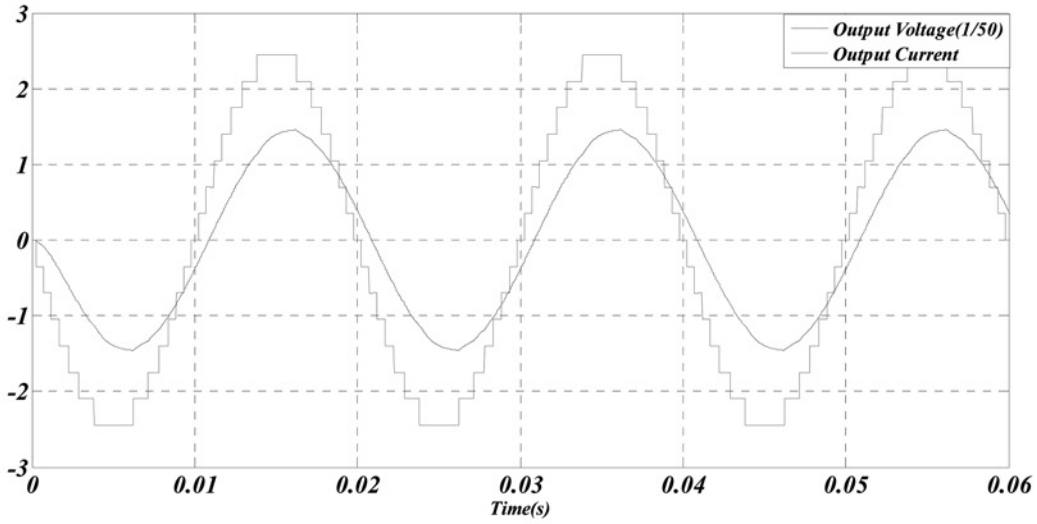

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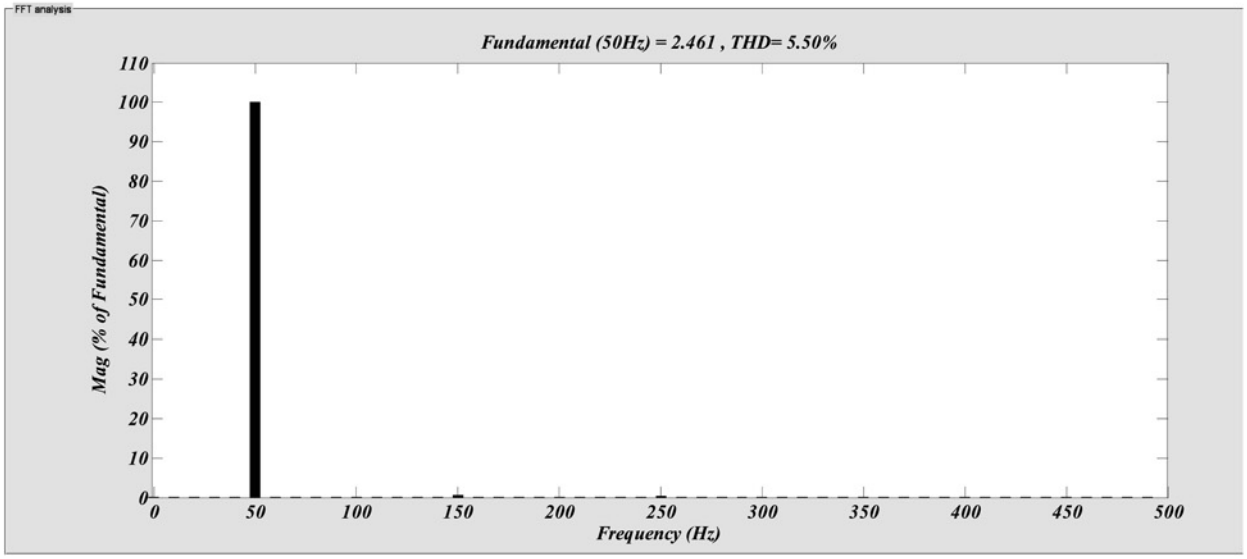

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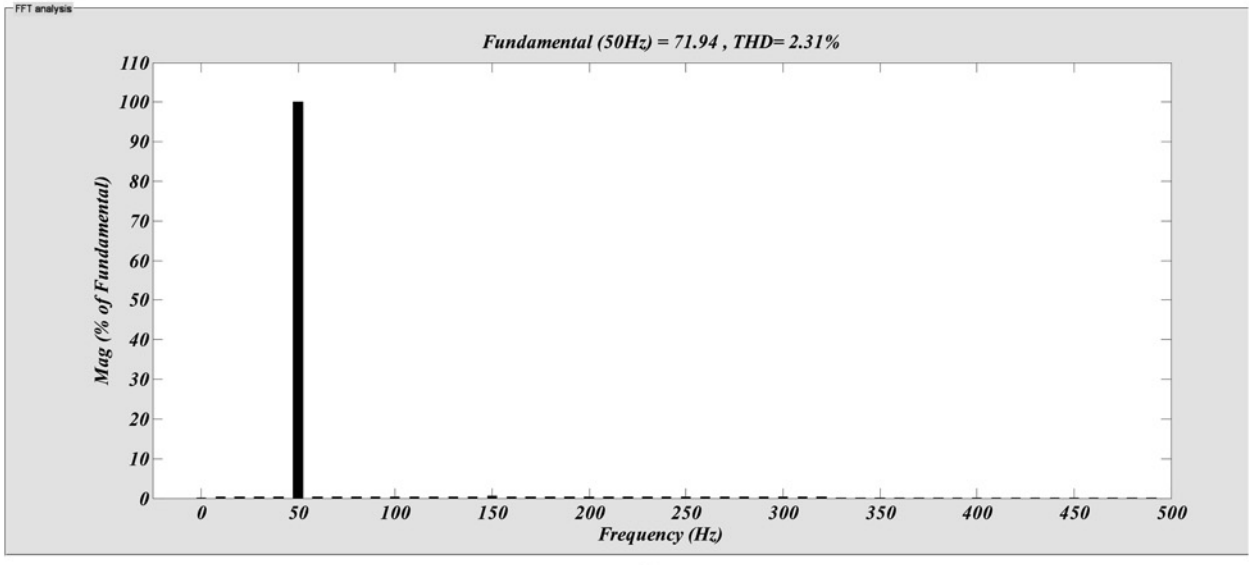

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Fig. 8 *Simulation results of fifteen-level proposed asymmetric topology*

a Output current and load voltage
b Harmonic spectrum of output current
c Harmonic spectrum of load voltage

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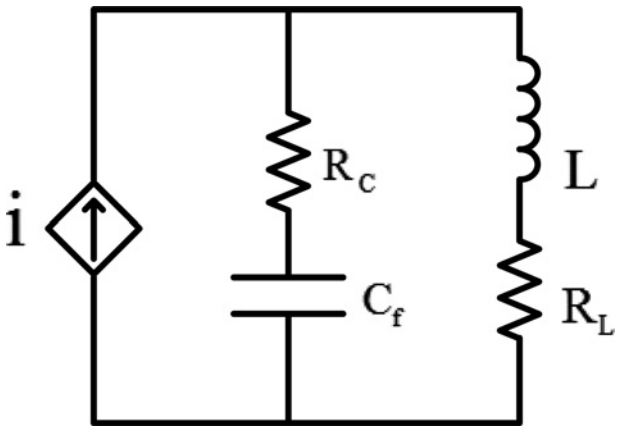

Fig. 9 *Output stage of CSI*

The index Anti-D points the parameter relevant to the anti-parallel diodes [5]. The switching losses are related to the switching frequency and the modulation approach. Finally, the total switching power losses can be calculated as below

$$P_{\text{sw}} = \sum_{1}^{i} P_{\text{sw},T_i} + P_{\text{sw,Anti-D}_i} \tag{20}$$

where i is the number of power switches.

Using (17) and (20), the total losses of the multilevel converter will be calculated as follows

$$P_{\text{loss}} = P_{\text{sw}} + P_{\text{C}} \tag{21}$$

It should be noted that the proposed inverter does not require any series diode in the structure, if the IGBT without anti-parallel diode is used. In the power loss calculation, for all compared structures, the series diode with IGBT is not considered. Consequently the losses related to the diodes will be equal to zero in the presented and conventional structures.

In addition, for all compared structures, only the inverter power losses are considered and in the analysis, the losses of the current source are not considered. Due to the lower number of current sources in proposed structures compared to other topologies, the losses of DC current source including IGBT, and inductor has lower influence on the efficiency of proposed topologies respect to other structures. Comparison of the power losses for the proposed symmetric and conventional structures is represented in Fig. 10. Calculation of losses is analysed based on sinusoidal PWM approach. For power losses calculation in the proposed converter, CHB and [15], the given parameters at datasheet of are simulated using BUP314 IGBT is used [19].

It is clear that power losses of the proposed structure would be lower in compared with CHB inverter and [15] due to lower number of IGBTs and lower number of on-state switches.

Clearly, the rating of devices in the reduced switched topologies is more than conventional one's. However, the ratings of power devices in low and medium power applications are almost same. Consequently, the number of required power switches is more important than the rating of power semiconductor switches in low/medium power applications. Regarding to the advantages of the proposed inverter, a bit increase in the total SDP of overall system as shown in Fig. 10*d* can be neglected where a considerable reduction in switches is achieved.

3.2 Asymmetric topologies

The proposed asymmetric topology is compared with the topology presented in [16] and the asymmetric CHB. The number of IGBTs

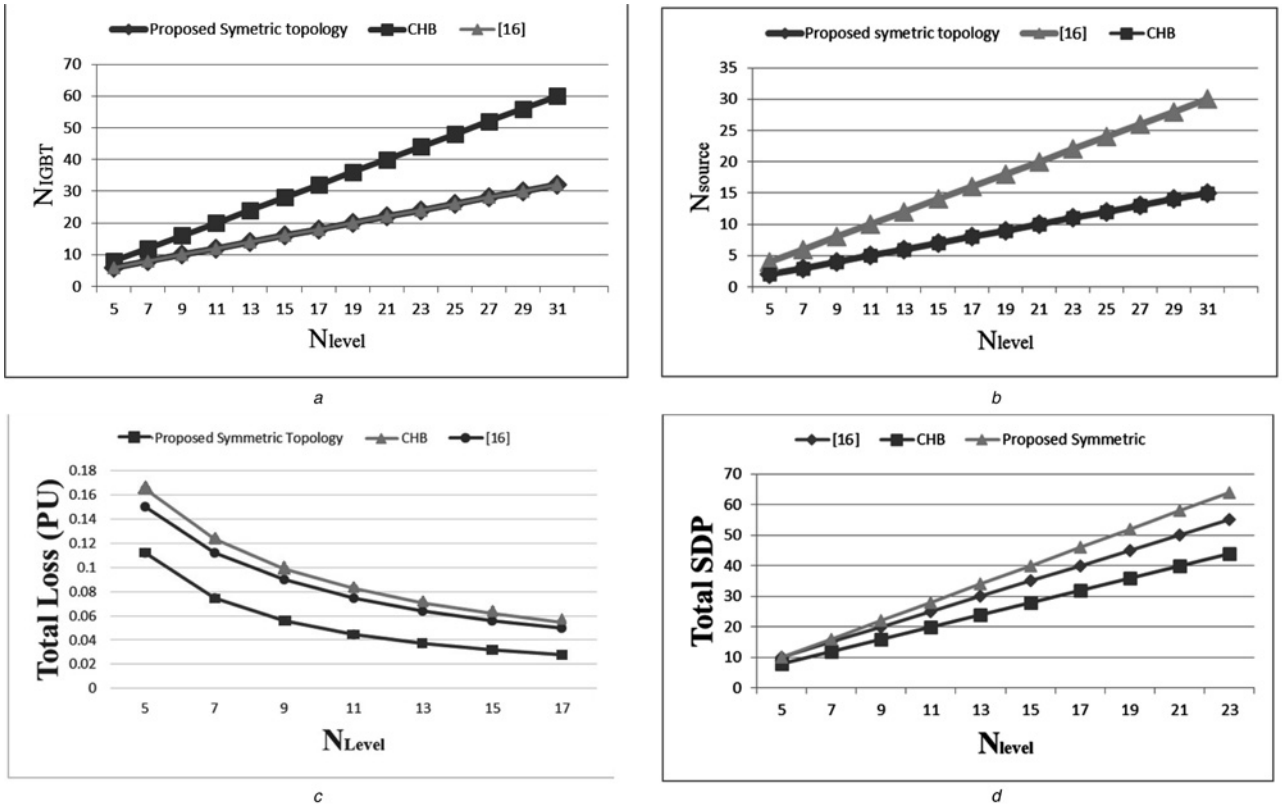

Fig. 10 *Comparison study between symmetric proposed topology and related topologies*

a Number of IGBTS
b Number of sources
c Total power losses
d Total switch device power

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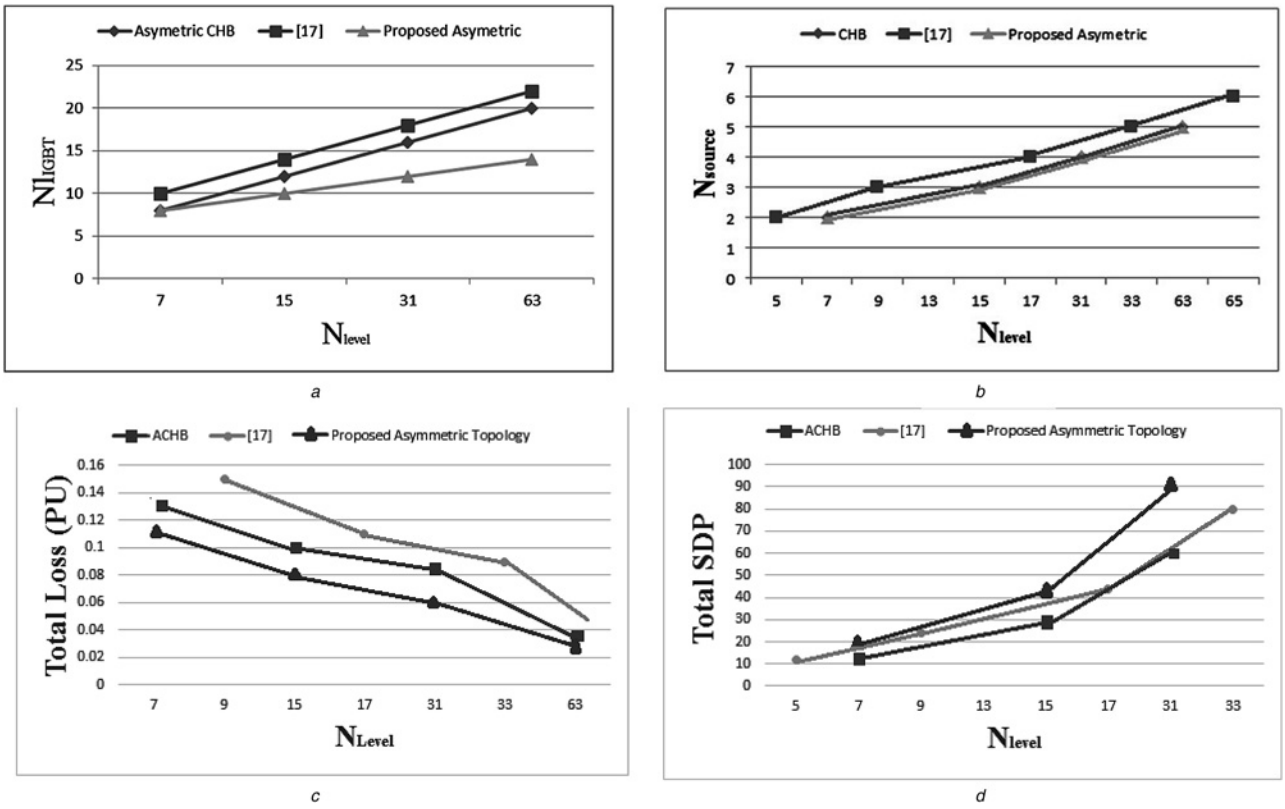

Fig. 11 *Comparison study between asymmetric proposed topology and related topologies*

a Number of IGBTS
b Number of sources
c Total power losses
d Total switch device power

versus the number of current levels is shown in Fig. 11*a*. This figure shows that the proposed inverter needs to lower the number of IGBTs. Figs. 11*b–d* show the number of sources, total power loss and total SDP, respectively. Similar to symmetric mode, the number of sources in the proposed topology and CHB are equal and lower than [16]. The other aspect which has to be compared, is the total losses. Considering Fig. 11*c*, due to lower number of on-state switches in current path, the proposed asymmetric topology has lower total losses compared to asymmetric CHB and [16]. However, the total SDP of the asymmetric CHB topology is lower than all of the topologies, the number of IGBTs reduced significantly in the proposed structure. In low/medium power converters, the number of IGBTs determines the cost of converter.

In order to get a better understanding, Table 4 illustrates a summarised comparison between the conventional symmetric and asymmetric CHBs [15–17] and the proposed topologies in symmetric and asymmetric forms. To compare fairly and rational, it is required to determine the number of levels (N) for all topologies.

4 Experimental results

In order to validate the practicability of the proposed configurations, a single-phase prototype of symmetric seven-level and asymmetric fifteen-level MSCI is implemented. Fig. 12 depicts the experimental results of the symmetric seven-level and asymmetric fifteen-level topologies which uses eight and ten IGBTs, respectively. The IGBT BUP 314 (without anti-parallel diode) is used as a power switch in the laboratory prototypes. The switches are driven using TLP250 and the gate signals are produced with a data acquisition card (PCI-1716) in the fundamental frequency. Moreover, similar to simulations, the load is $30 + j3.14\ \Omega$ and the output filter capacitor is 40 μF.

For symmetric topology, output current and load voltage are shown in Fig. 12*a*. As seen from this figure, all possible levels with the maximum value of 2.1 A are archived using the proposed converter.

The magnitude of input current sources, as shown in Fig. 12*b*, are regulated in desired values (0.7 A).

In order to generate all possible levels in asymmetrical topology, the input current should be regulated in the suitable values: 0.35, 0.7,

Table 4 Summarised comparison between proposed and conventional topologies in symmetrical and asymmetrical modes

MCSI topology	Number of IGBTs	Number of DC current sources	Number of inductors
symmetrical CHB	$2N–2$	$(N–1)/2$	$(N–1)/2$
asymmetrical CHB	$4[\text{Log}_2(N+1)-1]$	$\text{Log}_2(N+1)-1$	$\text{Log}_2(N+1)-1$
common-emitter MCSI topology [16]	$N+1$	$N-1$	$N-1$
inductor cell topology [17]	$4[\text{Log}_2(N-1)-1]+4$	1	$\text{Log}_2(N-1)-1$
CML topology [18]	$4[\text{Log}_2(N-1)-1]+4$	1	$2[\text{Log}_2(N-1)-1]$
symmetrical proposed MCSI	$N+1$	$(N–1)/2$	$(N–1)/2$
asymmetrical proposed MCSI	$2[\text{Log}_2(N+1)+1]$	$\text{Log}_2(N+1)-1$	$\text{Log}_2(N+1)-1$

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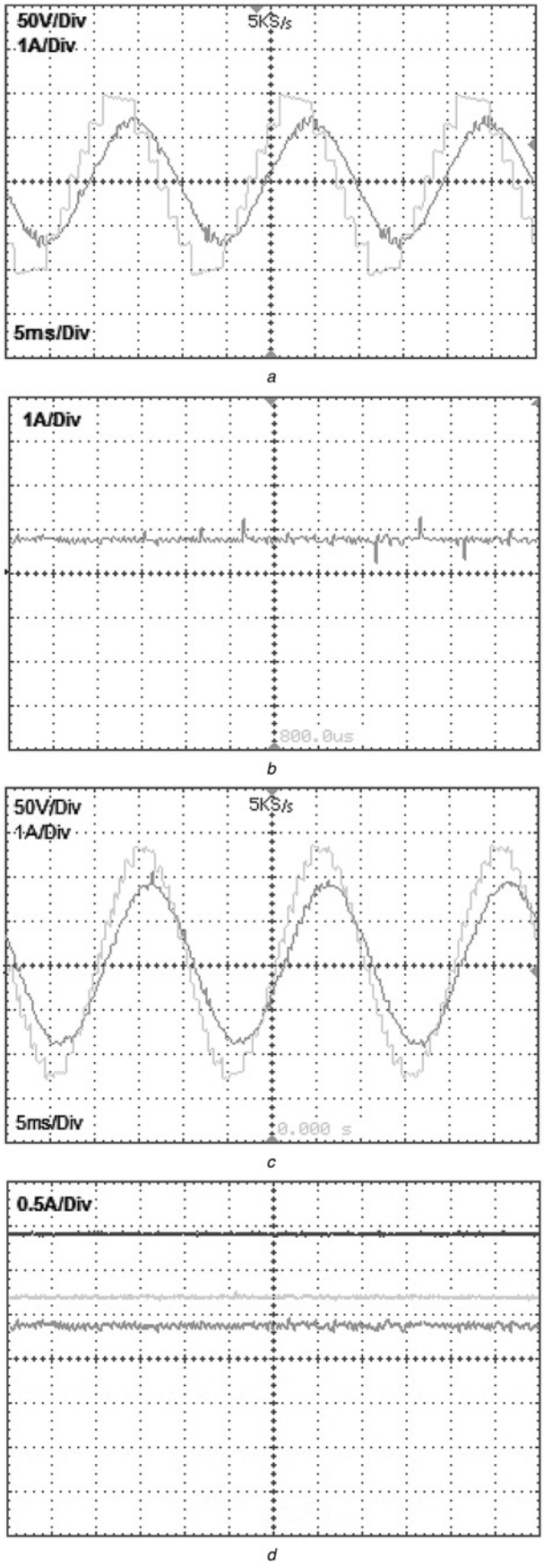

Fig. 12 *Experimental results of the symmetric seven-level and asymmetric fifteen-level topologies*

a Output current and load voltage of seven-level improved symmetric topology
b Current of each sources in symmetric mode
c Output current and load voltage of fifteen-level asymmetric topology
d Current of sources in asymmetric mode

and 1.4 A as shown in Fig 12*d*. In addition, the load voltage and output current are shown in Fig. 12*c*.

5 Conclusion

In this paper, new symmetric and asymmetric multilevel current source topologies are proposed. The proposed CSI uses a reduced number of devices compared to conventional structures. Also, it needs a lower number of DC current sources, switches, and gate driver circuits. A lower number of required devices lead to the reduction of the total implementation cost of converter. In addition, the implementation and control will be simple. The proposed inverter is compared with CHB and a recently proposed converter and the comparison results validate the features of proposed structures. A prototype of the proposed symmetric and asymmetric topologies has been constructed and all of the experimental results confirm the theoretical findings.

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